2021

(July)

COMPUTER SCIENCE

(Elective/Honours)

(Digital Logic Design and Computer Architecture)

(CS–201T)

Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **one** question from each Unit

UNIT—I

1. *(a)* Subtract the following decimal numbers by using either 9's complement or 10's complement : 1

3570 2100

(b) Subtract the following decimal numbers by using either 9's complement or 10's complement : 2

2100 3570

(c) Subtract the following binary numbers by using either 1's complement or 2's complement : 1

1100 1000

(d) Subtract the following binary numbers by using either 1's complement or 2's complement : 2

1000 1100

(e) Convert the following binary number to base 10 (decimal) : 1

$(1011)_2$

(f) Convert the following decimal number to base 8 (octal) : 1

$(15)_{10}$

(g) Convert the following binary number to base 10 (decimal) : 1

$(10.1)_2$

(h) Convert the following hexadecimal number to base 2 (binary) : 1

$(12AB)_{16}$

(i) Obtain the 9's complement of the following decimal number : 1

$(1234)_{10}$

(j) Convert the following hexadecimal number to base 10 (decimal) : 2

$(2B)_{16}$

(k) Obtain the 2's complement of the following binary number : 2

$(1000\,000)_2$

2. *(a)* Subtract the following decimal numbers by using either 9's complement or 10's complement : 1

5800 15

(b) Subtract the following decimal numbers by using either 9's complement or 10's complement : 2

15 5800

(c) Why are NAND and NOR gates considered universal gates? 2

(d) Explain the following in brief : 1×4=4

(i) 1's complement

(ii) 2's complement

(iii) 9's complement

(iv) 10's complement

(e) Use either 1's complement or 2's complement to perform the subtraction of the following binary numbers : 1

111 101

(f) Use either 1's complement or 2's complement to perform the subtraction of the following binary numbers : 1

101 111

(g) Explain the following in brief : 1×2=2

(i) Binary number system

(ii) Octal number system

(h) Find the 9's complement of the following decimal number : 1

$(9900)_{10}$

(i) Find the 2's complement of the following binary number : 1

$(1010101)_2$

UNIT—II

3. *(a)* Simplify the following Boolean expression, given by the function $F(A, B, C, D)$:

$F(A, B, C, D)$ $(1, 2, 3, 5, 6, 7, 13, 14, 15)$

Use a four-variable Karnaugh map. Write the simplified answer in the sum-of-products (SOP) form. 5

(b) Express the following Boolean expression as a sum of minterms : 2

$F(A, B, C)$ 1

(c) Use Don't care conditions to simplify the following :

$F(X, Y, Z)$ (1, 3, 4, 5, 7)

Don't care condition $d(X, Y, Z)$ (0, 6)

Make use of a three-variable Karnaugh map. Write the simplified answer in the sum-of-products (SOP) form. 5

(d) Draw a logic diagram using only NAND gates to represent the following Boolean expression : 2

$A.B \quad C.D$

(e) What is De Morgan's theorem? 1

4. *(a)* Define canonical form. 1

(b) Define Don't care condition. 1

(c) Use AND gates and OR gates to draw a logic diagram for the following Boolean expression : 2

$(W \quad X) \ (Y \quad Z)$

(d) Convert the following Boolean expression into its canonical form : 3

$F(A, B, C, D) \quad AB\ D \quad BCD$

(e) Explain, in brief, the following terms. Also use an example for each : (1+1)×4=8

(i) Minterm

(ii) Maxterm

(iii) Sum-of-products (SOP)

(iv) Product-of-sums (POS)

UNIT—III

5. *(a)* Show the step-by-step multiplication process using Booth's algorithm for multiplying the following numbers, where both of the given numbers are positive :

(15) (13)

Assume that all of the registers used are of size 5 bits each. 10

(b) Make the truth table of a full-adder, with X, Y and Z as the three inputs. Use C as the output for the Carry. Also use S as the output for the Sum. 3

(c) How is Logical Shift Right different from Logical Shift Left? 2

6. *(a)* Draw the flowchart of Booth's algorithm for multiplying two binary integers in 2's complement representation. 4

(b) Explain the hardware used for Booth's algorithm with a diagram. 7

(c) What is a half-adder? Explain with the help of a diagram. 4

UNIT—IV

7. *(a)* With the help of a block diagram, explain the working of a *J-K* flip-flop. How is a race condition overcome? 6+2=8

(b) What is a register? 1

(c) What is a counter? 1

(d) Explain the following two terms, with respect to a flip-flop : 1×2=2

(i) Present state

(ii) Next state

(e) What is an indeterminate state of an *R-S* flip-flop? 1

(f) Explain, in brief, the following addressing modes with examples : 1×2=2

(i) Direct addressing mode

(ii) Indirect addressing mode

8. Design a 3-bit counter. It goes through the following eight states, expressed as 3-bit numbers, namely, 000, 001, 010, 011, 100, 101, 110 and 111 in binary, (i.e., 0, 1, 2, 3, 4, 5, 6 and 7 in decimal). Make use of any type of flip flops for the design of the counter.

Answer the following :

(a) Draw the state diagram for the above counter.

(b) Derive the excitation table for the above counter. 3+12=15

UNIT—V

9. *(a)* What do you mean by hit ratio in a cache memory? 2

(b) Draw a diagram that shows how four 128 8 RAMs can be connected to the CPU. 4

(c) Explain the following with reference to the cache memory : 3+4=7

(i) Direct mapping

(ii) Set-associative mapping

(d) Explain the concept of locality of reference with respect to cache memory. 2

10. *(a)* Explain DMA transfer with the help of a diagram. 6

(b) Differentiate between cycle stealing and burst transfer. 3

(c) Explain the following modes of data transfer : 3+3=6

(i) Programmed I/O mode of a data transfer

(ii) Interrupt-initiated mode of a data transfer

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