2022

(May/June)

COMPUTER SCIENCE

(Elective/Honours)

(Digital Logic Design and Computer Architecture)

(CS–201T)

Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **five** questions, selecting **one** from each Unit

UNIT—I

1. *(a)* Subtract the following decimal numbers by using 9's complement : 1

357 – 210

(b) Subtract the following decimal numbers by using 9's complement : 2

21 – 37

(c) Subtract the following binary numbers by using 1's complement : 1

110 – 100

(d) Subtract the following binary numbers by using 1's complement : 2

100 – 110

(e) Convert the following binary number to base 10 : 1

1111

(f) Convert the following binary number to base 8 : 1

1111

(g) Convert the following binary number to base 10 : 1

1.1

(h) Convert the following hexadecimal number to base 2 : 1

AB

(i) Convert the following hexadecimal number to base 10 : 2

B2

(j) Obtain the 9's complement of the following decimal number : 1

12

(k) Obtain the 2's complement of the following binary number : 2

10

2. (a) Subtract the following decimal numbers by using 9's complement : 1

580 – 5

(b) Subtract the following decimal numbers by using 9's complement : 2

18 – 47

(c) Why is NAND called as a universal gate? 2

(d) Explain the following logic gates in brief : 2×2=4

(i) AND

(ii) OR

(e) Subtract the following binary numbers by using 1's complement : 1

110 – 100

(f) Subtract the following binary numbers by using 1's complement : 1

100 – 110

(g) Draw the truth table of a 2-input EX-OR gate. 2

(h) Obtain the 9's complement of the following decimal number : 1

99

(i) What is the 1's complement of the binary number 10? 1

UNIT—II

3. (a) Simplify the following : 5

$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 12, 13, 14, 15)$

(b) Express the following as a product of maxterms : 2

$(XY + Z)(X + YZ)$

(c) Use the given Don't Care conditions $d(A, B, C, D)$ to simplify the following :

$F(A, B, C, D) = \Sigma(0, 1, 2, 6, 10, 14)$
$d(A, B, C, D) = \Sigma(3, 7, 11, 15)$

Make use of a Karnaugh map. 5

(d) Draw a logic diagram for the expression $AB + C$ using only NAND gates. 2

(e) What is De Morgan's theorem? 1

4. (a) Define canonical form. 2

(b) What is a Don't Care condition? 1

(c) Given an expression $(A + B)C$, use logic gates to draw its logic diagram. 2

(d) Given an expression $AC + BD$, derive its canonical form. 2

(e) Explain the following in brief : 2×4=8

(i) Sum of Products

(ii) Product of Sums

(iii) Minterm

(iv) Maxterm

UNIT—III

5. (a) Use Booth's algorithm to perform the multiplication $(-15) \times (+13)$. Assume that size of the registers is 5 bits. 12

(b) Draw the truth table of a half adder. 2

(c) Derive the expression for the sum of a half adder. 1

6. (a) Draw the flowchart of Booth's algorithm. 7

(b) The contents of a 4-bit register A is 1101.

Show the contents of the register A after one logical left shift. 2

(c) Explain the following in brief : 2×3=6

(i) Logical Left Shift

(ii) Arithmetic Left Shift

(iii) Arithmetic Right Shift

UNIT—IV

7. Use T flip-flops to design a counter that counts 0, 1, 2, 3, 4, 5, 6, 7.

Answer the following with respect to this counter :

(a) Draw the state diagram. 1

(b) Derive the excitation table. 5

(c) Use the above excitation table to draw three separate Karnaugh maps. 3

(d) Use the above Karnaugh maps to derive three input equations. 3

(e) Draw a logic diagram for the above counter. 3

8. (a) Explain the following in brief : 2×2=4

(i) Flip-flop

(ii) Addressing mode

(b) Fill in the following truth table for SR Flip-Flop using NAND gates :

S	R	Q^t	Q^{t+1}
0	0	—	—
0	1	—	—
1	0	—	—
1	1	—	—

where Q^t is the present state and Q^{t+1} is the next state. 4

(c) Explain indirect addressing mode. 2

(d) Draw the characteristic table of T-flop. 2

(e) Draw the excitation table of D-flop. 3

UNIT—V

9. Explain the following three modes of input/output transfer : 5×3=15

(a) Programmed I/O

(b) Interrupt Initiated I/O

(c) Direct Memory Access (DMA)

10. (a) Explain the following in brief : 2×2=4

(i) Primary memory

(ii) Secondary memory

(b) Explain the following in brief : 2×2=4

(i) Associative mapping

(ii) Direct mapping

(c) What is set-associative mapping? Explain. 3

(d) What is 'Hit Ratio'? 1

(e) Explain 'locality of reference'. 2

(f) Why is associative memory also called as content addressable memory (CAM)? 1

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