2019

(April)

COMPUTER SCIENCE

(Elective/Honours)

(Digital Logic Design and Computer Architecture)

(CS–201T)

Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **one** question from each Unit

UNIT—I

1. *(a)* Subtract the following decimal numbers using 9's complement : 1

9876 – 1234

(b) Subtract the following decimal numbers using 9's complement : 2

1234 – 9876

(c) Subtract the following binary numbers using 1's complement : 1

$$110 - 101$$

(d) Subtract the following binary numbers using 1's complement : 2

$$101 - 110$$

(e) Convert the following binary number to decimal : 2

$$(1000)_2$$

(f) Convert the following decimal number to octal : 1

$$(120.625)_{10}$$

(g) Convert the following binary number to decimal : 1

$$(1110101.110)_2$$

(h) Convert the following hexadecimal number to binary : 1

$$(306.D)_{16}$$

(i) Convert the following hexadecimal number to decimal : 2

$$(BADA)_{16}$$

(j) Obtain the 2's complement of the following binary number : 1

$$(00\ 00\ 001)_2$$

(k) Obtain the 9's complement of the following decimal number : 1

$$(0\ 9900)_{10}$$

(Continued)

2. (a) Subtract the following by using 9's complement : 1

$$5 - 2$$

(b) Subtract the following by using 9's complement : 1

$$2 - 5$$

(c) Convert the following decimal number to binary : 2

$$(9)_{10}$$

(d) How can a negative number be represented in 2's complement? Explain with an example. 2+2=4

(e) Explain, in brief, all of the following gates : 1×6=6

(i) AND gate

(ii) OR gate

(iii) NAND gate

(iv) NOR gate

(v) EX-OR gate

(vi) EX-NOR gate

(f) Draw the truth table of a 2-input EX-OR gate. 1

(Turn Over)

UNIT—II

3. *(a)* The following is a boolean function $F(A, B)$. Express the function $F(A, B)$ as a sum of minterms : 1

$$F(A, B) = 1$$

(b) Use a 4-variable Karnaugh map to simplify the following boolean function : 4

$$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 12, 13, 14, 15)$$

(c) *(i)* Simplify the following boolean function $F(A, B, C, D)$: 3

$$F(A, B, C, D) = A'B'C'D' + A'B'C'D + A'BCD' + A'BCD + AB'CD' + AB'CD + ABC'D' + ABC'D$$

(ii) Use any type(s) of logic gates, of your choice, to draw the logic diagram of the above simplified expression. 3

(d) Use a Karnaugh map of four variables to simplify the following function $F(A, B, C, D)$. A Don't Care condition $d(A, B, C, D)$ is also given. Write the answer in the SOP (Sum-Of-Products) form : 4

$$F(A, B, C, D) = \Sigma(0, 1, 2, 6, 10, 14)$$

$$d(A, B, C, D) = \Sigma(3, 7, 11, 15)$$

(Continued)

4. *(a)* What is De Morgan's theorem? 1

(b) Explain, in brief, the following terms. Also use an example for each : (1+1)×4=8

(i) Minterm

(ii) Maxterm

(iii) Sum-Of-Products (SOP)

(iv) Product-Of-Sums (POS)

(c) What is a Don't Care condition? 1

(d) Convert the following boolean function $F(A, B, C, D)$ to its canonical form : 3

$$F(A, B, C, D) = AC' + BC + BD'$$

(e) Express the following boolean function $F(X, Y, Z)$ as a sum of maxterms : 2

$$F(X, Y, Z) = (XY + Z) \cdot (X + YZ)$$

UNIT—III

5. *(a)* Show the step-by-step multiplication process using Booth's algorithm for multiplying the following numbers, where one is a negative number (minus 15) and the other is a positive number (plus 13). Assume that all the registers used are of size 5 bits each : 10

$$(-15) \times (+13)$$

(Turn Over)

(b) (i) Draw the truth table of a Full Adder (FA). Use the three variables X, Y and Z as the three inputs; and variables S and C for the Sum and the Carry respectively. 2

(ii) Derive the two Boolean expressions for the Sum S and Carry C, for the above Full Adder. 1+1=2

(c) The content of a 4-bit register A is initially 1101. Show the content of the register A after one logical left shift has been performed. 1

6. (a) Explain the following types of adders : 3+4=7

(i) Half Adder (HA)

(ii) Full Adder (FA)

(b) Explain the following : 2×4=8

(i) Logical left shift

(ii) Logical right shift

(iii) Arithmetic left shift

(iv) Arithmetic right shift

(Continued)

UNIT—IV

7. Use three T flip-flops named as A, B and C to design a 3-bit counter that counts eight states, namely, from the state zero to the state seven; that is, the values of A, B and C in binary are 000, 001, 010, ... up to 110, 111. After the last state 111, the counter will repeat itself to the beginning state 000. And then the same sequence will be repeated as 000, 001, 010, ... up to 110, 111. Answer the following with respect to the design of this counter :

(a) Draw the state diagram. 1

(b) Derive the excitation table. 5

(c) Use the above excitation table to draw the three different Karnaugh maps. 3

(d) Use the above Karnaugh maps to derive the three flip-flop input equations. 3

(e) Draw the logic diagram for the above counter by using the three T flip-flops A, B and C; and if necessary, use any logic gate(s). 3

8. (a) Explain the following, in brief : 2×3=6

(i) Flip-flop

(ii) Instruction cycle

(iii) Addressing mode

(Turn Over)

(b) Explain the following, in brief : 1×4=4

(i) Present state PS Q(t) in a flip-flop

(ii) Next state NS Q(t+1) in a flip-flop

(iii) Register

(iv) Direct addressing mode

(c) Explain indirect addressing mode. 2

(d) Draw the characteristic table of any flip-flop. 2

(e) Draw the excitation table of any flip-flop. 1

UNIT—V

9. Explain the following three modes of transfer : 5×3=15

(a) Programmed I/O

(b) Interrupt-initiated I/O

(c) DMA

10. (a) Explain the following : 2×2=4

(i) Primary memory

(ii) Secondary memory

(Continued)

(b) Explain, in brief, of the following three mappings used in cache memory : 2×3=6

(i) Associative mapping

(ii) Direct mapping

(iii) Set-associative mapping

(c) What is 'hit ratio'? 1

(d) Explain 'locality of reference' (LOR) with respect to cache memory. 2

(e) Draw the block diagram of a RAM. 1

(f) Why is associative memory called as 'CAM' (Content Addressable Memory)? 1

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